

AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning at page 13, line 2, with the following rewritten paragraph.

-- Initially, an explanation will be given on a first test which evaluates a desired subject address by narrowing the cycle period rate of the test pattern relative to the subject address. FIG. 2 is a timing chart of the first test executed in the semiconductor testing apparatus which represents an embodiment of the present invention. This timing chart shows a case of narrowing the cycle period rate where, out of the partial test pattern ranging from an (N)-th address to an (N+4)-th address in an arbitrary address section, an (N+3)-th address is designated as a specific subject address. In this case, the cycle period rate of the entire test pattern is set to a value (RATE 1) lower than the maximum operation frequency and, in conformity with the set information, the rate of the specific subject address only, i.e., the (N+3)-th cycle, is raised to a higher value (RATE 2). As a result, there occurs a state where the timing of each signal only in the specific subject address of the (N+3)-th cycle restricts the operation of the device. Thus, it becomes possible to evaluate the timing power and the margin of the subject address without being affected by the timing of any other address. And the cycle frequency rate of the specific address can be successively narrowed by changing the set information, hence realizing confirmation of the maximum operation frequency in the relevant portion. --